Notice of Allowability	Application No.	Applicant(s)	
	10/023,819	CHANDRAN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed 17 Jul 2006*.

2. ☒ The allowed claim(s) is/are *1-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 07-17-2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

John B. Vigushin
Primary Examiner
Art Unit: 2841

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on July 17, 2006 has been entered.

Allowable Subject Matter

2. Claims 1-29 have been allowed.

3. The following is an examiner's statement of reasons for allowance:

As to Claims 1-9, patentability resides in *thermally expanding each of the semiconductor chip and substrate substantially the same amount in a direction along surfaces thereof to be joined by soldering*, in combination with the other limitations of base Claim 1.

As to Claims 10-13, patentability resides in *thermally expanding each of the first and second members substantially the same amount in a direction along surface thereof to be joined*, in combination with the other limitations of base Claim 10.

As to Claims 14-16, 20, 21 and 22-24, 28, 29, patentability resides in the limitation wherein *the magnitude of the elongation mismatches and the stresses*

induced thereby in the electronic assembly are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints, in combination with the other limitations of base Claims 14 and 22, respectively.

As to Claims 17-19 and 25-27, patentability resides, at least in part, in *the limitation wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements*, in combination with the other limitations of base Claims 17 and 25, respectively.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Claims 1-16, 20, 21, 17-19, 22-24, 28, 29 and 25-27 of the instant allowed Application will be renumbered as Claims 1-29, respectively, for publication in the issued patent.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. *Examiner's Note*: All prior art cited below has been made of record in Applicant's IDS filed July 17, 2006.

a) (i) Kajiwara et al. (US 6,798,072 B2) discloses: a substrate 4 having a first CTE (20 ppm/°C; col.12: 64-col.13: 4); a semiconductor (silicon) chip 1 (col.19: 23)

having a second CTE (not explicitly recited) different than the first CTE (the CTE difference between chip 1 and board 4 is recognized by Kajiwara et al. in col.8: 57-65, col.12: 15-20, col.12: 64-col.13: 4 and col.20: 67-col.21: 9); a plurality of soldered joints {i.e., Au bumps 3 of chip and the Sn plating 130 of Cu pads 5 on substrate 4 form a Au-Sn low melting point eutectic alloy upon heating, thus forming Au-Sn (which constitutes a solder alloy) fillets (Fig. 13; col.17: 26-49 and col.19: 1-8)} connecting chip 1 and substrate 4 (Fig. 13); wherein chip 1 and substrate 4 across the plurality of soldered joints of the assembly at room temperature have CTE difference induced elongation mismatches and stresses induced thereby in the electronic assembly from soldering (col.8: 55-65; col.12: 15-20; col.12: 64-col.13: 4; col.19: 1-16); wherein a magnitude of the elongation mismatches and the stresses induced thereby in the electronic assembly is less than that expected based upon cooling the substrate 4 and the chip 1 from a solder solidification temperature to the room temperature following soldering of the plurality of soldered Au-Sn joints (col.8: 55-65 describes prior art problem and col.12: 15-20 indicates the apparatus and method disclosed that cures the problem; see also embodiments that utilize this disclosed apparatus and method in col.16: 61-col.17: 22 and col.19: 1-16).

(ii) As indicated above, Kajiwara et al. discloses a reduced magnitude of the elongation mismatch between chip 1 and substrate 4 based upon cooling the substrate and chip from a solder solidification temperature to the room temperature but does not offer a specific range of reduction; i.e., does not explicitly teach that the magnitude of the elongation mismatches is **less than one-half** that expected based

upon cooling the substrate and chip from a solder solidification temperature to the room temperature. Kajiwara et al. teaches a joining process and apparatus wherein "the temperature on the board side is made equal to or lower than that on the chip side, whereby the generation of the thermal strain in the cooling process can be reduced" (col.12: 15-17) and provides at least one embodiment where thermal strain in the cooling process has been so reduced (col.18: 55-col.19: 16). However, Kajiwara et al. does not indicate the extent of reduction in thermal strain, due to the elongation mismatch, that is contemplated as sufficient for the application. Is the elongation mismatch due to CTE mismatch between chip and board reduced by 40%, 50%, greater than 50%? This is not readily ascertainable from the general range of board temperatures of less than or equal to the chip temperature, as recited in Kajiwara et al. (col.12: 15-17), with no specific pair of temperatures cited for the chip and board, respectively; and Kajiwara et al. does not fairly suggest in the disclosed apparatus and method that, in order for the final product assembly to be reliable, the elongation mismatch must be less than one-half that expected based upon cooling the substrate and chip from a solder solidification temperature to room temperature, as required by Applicant's product Claims 14, 17, 22 and 25; rather the thermal strain between the chip and board during the cooling process is only generally recited as "reduced," and as mentioned above, no relationships of temperature between chip and board, which would provide information comparing their respective dimensional expansion (and contraction) during the joining process, are ever taught in Kajiwara et al.

(iii) Also, Kajiwara et al. teaches a joining process and apparatus wherein "the temperature on the board side is made equal to or lower than that on the chip side, whereby the generation of the thermal strain in the cooling process can be reduced" (col.12: 15-17) but does not teach or fairly suggest a specific relationship between board temperature and chip temperature whereby the board and chip thermally expand "substantially a same amount in a direction along surfaces thereof to be joined by soldering," as required in process Claims 1 and 10.

b) Cobbley et al. (US 6,689,635 B1) discloses a die 30 pre-heated to promote adhesion to polymer bumps 22 of substrate 10 (col.4: 56-65; col.5: 18-22).

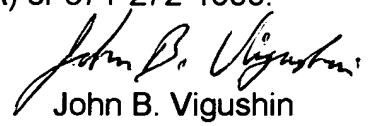
c) Wang et al. (US 6,365,435 B1) discloses a substrate 10 to which a die 40 is mounted, wherein the joining process comprises pre-heating substrate 10 (col.4: 11-21), then pre-heating die 40 (col.4: 22-30), and then heating the substrate/die assembly (col.4: 36-40) in order to reduce the amount of air trapped by the underfill 5 (col.4: 31-35 and 41-45).

d) Kubota et al. (US 2002/0140094 A1) discloses a thermo-compression bonding process comprising rapid heating of a chip 325 to reflow solder bumps 305 of the substrate 315 to which the chip 325 is being mounted (paragraph [0025]).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
September 03, 2006